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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/693,987	10/23/2000	Hiroyuki Kawamoto	198574US2	9308

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EXAMINER	
LAMB, TWYLER MARIE	

ART UNIT	PAPER NUMBER
2622	

DATE MAILED: 10/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/693,987	Applicant(s) KAWAMOTO ET AL.	
	Examiner Twyler M. Lamb	Art Unit 2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 5-7 and 9-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Tomassi et al. (Tomassi) (US 5,606,707).

With regard to claim 1, Tomassi discloses an image processing apparatus (Figure 1, real-time image processor 101) which refers to peripheral pixels of a target pixel to perform processing of said target pixel (col 34, lines 50-52), said image processing apparatus comprising: an input I/F memory (IBIB FIFO 211, OBIB FIFO 213) which reads pixels having a predetermined length, subjects these pixels to buffering (col 8, lines 9-20), and then writes these pixels in a SIMD type processor (SIMD array 201, col 8, lines 9-20); a SIMD type processor (SIMD array 201) which performs batch processing of the pixels written from said input I/F memory (col 8, lines 9-20); an output I/F memory (OBOB FIFOI 217) which reads the pixels batch-processed by said SIMD type processor, subjects the pixels to buffering and writes the pixels in a predetermined

output destination (col 8, lines 21-27); and a control unit (OBAG 205) which controls the read and/or write timing of said input I/F memory and said output I/F memory (col 8, lines 53-65; col 11, lines 50-54).

With regard to claims 2, 6 and 10, Tomassi also discloses wherein said control unit controls the write and/or read timing to thereby use said input I/F memory and output I/F memory a plurality of times (col 11, line 50 – col 12, line 17).

With regard to claims 3, 7 and 11, Tomassi also discloses wherein an effective number of pixels obtained by subtracting the number of peripheral pixels referred to for said target pixel from the number of pixels batch-processed by said SIMD type processor is multiples in a dither matrix (col 7, lines 43-53).

With regard to claim 5, Tomassi discloses an image processing apparatus (Figure 1, real-time image processor 101) which refers to peripheral pixels of a target pixel to perform processing of said target pixel (col 34, lines 50-52), said image processing apparatus comprising: an input I/F memory (IBIB FIFO 211, OBIB FIFO 213) which reads pixels having a predetermined length, subjects these pixels to buffering (col 8, lines 9-20), and then writes these pixels in a SIMD type processor at a speed faster than when the pixels were read (SIMD array 201, col 8, lines 9-20); a SIMD type processor (SIMD array 201) which performs batch processing of the pixels written from said input I/F memory (col 8, lines 9-20); an output I/F memory (OBOB FIFOI 217) which reads the pixels batch-processed by said SIMD type processor, subjects the pixels to buffering and writes the pixels in a predetermined output destination at a speed slower than that of readout of said batch-processed pixels (col 8, lines 21-27); and a

control unit (OBAG 205) which controls the read and/or write speed of said input I/F memory and said output I/F memory (col 8, lines 53-65; col 11, lines 50-54).

With regard to claim 9, Tomassi discloses an image processing apparatus (Figure 1, real-time image processor 101) which refers to peripheral pixels of a target pixel to perform processing of said target pixel (col 34, lines 50-52), said image processing apparatus comprising: an input I/F memory (IBIB FIFO 211, OBIB FIFO 213) which reads pixels having a predetermined length, subjects these pixels to buffering (col 8, lines 9-20), and then writes these pixels in a SIMD type processor at a speed faster than when the pixels were read, and which has a capacity smaller than pixels batch-processed by said SIMD type processor (SIMD array 201, col 8, lines 9-20); a SIMD type processor (SIMD array 201) which performs batch processing of the pixels written from said input I/F memory (col 8, lines 9-20); output I/F memory (OBOB FIFOI 217) which reads the pixels batch-processed by said SIMD type processor, subjects the pixels to buffering and writes the pixels in a predetermined output destination at a speed slower than that of readout of said batch-processed pixels, and which has a capacity smaller than pixels batch-processed by said SIMD type processor (col 8, lines 21-27); and a control unit (OBAG 205) which controls the write and/or read speed with respect said input I/F memory, and the write and/or read timing with respect said input I/F memory based on said speed and the capacity of said input I/F memory, and/or the write and/or read speed with respect said output I /F memory, and the write and/or read timing with respect said output I/F memory based on said speed and the capacity of said output I/F memory (col 8, lines 53-65; col 11, lines 50-54).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 4, 8 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomassi et al. (Tomassi) (US 5,606,707) in view of Johnson (US 5,253,308).

With regard to claims 4, 8 and 12, Tomassi does not specifically teach wherein said SIMD type processor is physically detachable from said input I/F memory or said output I/F memory.

Johnson discloses an image data processor where defective elements can be remove that includes wherein said SIMD type processor is physically detachable from said input I/F memory or said output I/F memory (col 12, lines 6-21).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Tomassi to include wherein said SIMD type processor is physically detachable from said input I/F memory or said output I/F memory as taught by Johnson. It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Tomassi by the teaching of Johnson to provide fault tolerance as taught by Johnson in col 6, lines 36-48).

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Twyler Lamb whose telephone number is 703 - 308-8823. The examiner can normally be reached on M-TH (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward L Coles can be reached on 703-308-4712. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9306 for regular communications and 703-872-9314 for After Final communications.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, DC 20231

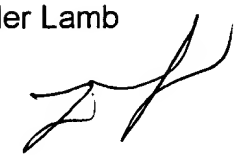
or faxed to:

(703) 872-9314
(for informal or draft communications, such as proposed amendments to be discussed at an interview; please label such communications "PROPOSED" or "DRAFT")

or hand-carried to:

Crystal Park Two
2121 Crystal Drive
Arlington. VA.
Sixth Floor (Receptionist)

Twyler Lamb



September 30, 2004